JFW

Docket No.: 4363P005C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

DAVID M. COLLERAN, ET AL.

Application No.: 10/810,444

Filed: March 26, 2004

For: **Automatic Phase Lock Loop Design Using Geometric Programming**

Art Group: TBA

Examiner: TBA

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed for applications filed after June 30, 2003). This IDS and IDS Citation Form are being submitted before the mailing of a first Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: July 23, 2004

Chui-Kiu Teresa Wong, Reg. No. 48,042

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Los Angeles, CA 90025
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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

07-23-04

Esther L. Campbell ***Date***

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	10/810,444
Filing Date	March 26, 2004
First Named Inventor	David M. Colleran
Art Unit	TBA
Examiner Name	TBA
Total Number of Pages in This Submission: 28	Attorney Docket Number: 4363P005C

ENCLOSURES ***(check all that apply)***

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ Information Disclosure Statement
  - ☒ PTO/SB/08
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Basic Filing Fee
  - ☐ Declaration/POA
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s)
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*

19 cited references and Return Receipt Postcard.

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Chui-Kiu Teresa Wong, Reg. No. 48,042 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	July 23, 2004

CERTIFICATE OF MAILING/TRANSMISSION

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Typed or printed name	**Esther L. Campbell**		
Signature		Date	**July 23, 2004**

Based on PTO/SB/21 (04-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wtr) 06/04/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

FEE TRANSMITTAL for FY 2004

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 0.00

Complete if Known	
Application Number	10/810,444
Filing Date	March 26, 2004
First Named Inventor	David M. Colleran
Examiner Name	TBA
Art Unit	TBA
Attorney Docket No.	4363P005C

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or underpayment of fees as required under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

☐ Charge fee(s) indicated below, **except for the filing fee** - to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	8	- 20* =	0	X	18.00	=	$0.00
Independent Claims	2	- 3* =	0	X	86.00	=	$0.00
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple Dependent claim, if not paid
1204	86	2204	43	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

***or number previously paid, if greater, For Reissues, see below*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1404	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Prosessing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	1809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Chui-Kiu Teresa Wong	Registration No. (Attorney/Agent)	48,042	Telephone	(408) 720-8300
Signature				Date	07/23/04

Based on PTO/SB/17 (10-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 02/10/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Substitute for Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known	
Application Number	10/810,444
Filing Date	March 26, 2004
First Named Inventor:	Dave Colleran
Art Unit	TBA
Examiner Name	TBA
Attorney Docket Number	4363P005C

Sheet	1	of	3

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-	6,311,145 B1	10/30/2001	Hershenson	
		US-	6,425,111 B1	7/23/2002	del Mar Hershenson	
		US-	6,577,992 B1	6/10/2003	Tcherniaev, et al.	
		US-	6,532,569 B1	3/11/2003	Christen, et al.	
		US-	6,381,563 B1	4/30/2002	O'Riordan, et al.	
		US-	4,827,428	5/2/1989	Dunlop, et al.	
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		US-				
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	10/810,444
				Filing Date	March 26, 2004
				First Named Inventor:	Dave Colleran
				Art Unit	TBA
				Examiner Name	TBA
Sheet	2	**of**	3	Attorney Docket Number	4363P005

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		KORTANEK, K.O., et al., "An Infeasible Interior-Point Algorithm For Solving Primal And Dual Geometric Programs," pp., 155-181, Mathematical Programming Society, Inc., 76:155-181, January 1, 1995.	
		GIELEN, G., et al., "An Analogue Module Generator For Mixed Analogue/Digital ASIC Design", International Journal of Circuit Theory and Applications, Vol. 23, pp. 269-283, 1995.	
		HERSHENSON, M., et al., "Automated Design of Folded-Cascode Op-Amps with Sensitivity Analysis", pp. 121-124, Electonrics, Circuits and Systems, IEEE International Conference on LISBOA, September 7-10, 1998.	
		HERSHENSON, M., et al., "Optimization of Inductor Circutis via Geometric Programming", pp. 994-998, Design Automation Conference, June 21, 1999, Proceddings.	
		MEDIERO, F., et al., "A Vertically Integrated Tool For Automated Design Of Sigma Delta Modulators", IEEE Journal of Solid-State Circuits, Vol. 30., No. 7, July 1, 1995, pp. 762-767.	
		HERSHENSON, M., et al., "Optimal Design Of A CMOS Op-Amp Via Geometric Programming", IEEE Transactions On Computer Aided Design Of Integrated Circuits And Systems, Vol. 20., N. 1 January 2001, pp. 1-21.	
		MANDAL, P., et al., "CMOS Op-Amp Sizing Using A Geometry Programming Formulation", IEEE Transactions On Computer Aided Design Of Integrated Circuits And Systems, Vol. 20., No. 1, January 31, 2001, pp. 22-38.	
		DAEMS, W., et al., "Simulation-based Automatic Generation Of Signomial And Posynomial Performance Models For Analog Integrated Circuit Sizing", IEEE/ACM International Conference On Computer-Aided Design, November 4, 2001, pp. 70-74.	
		VON KAENEL, V., et al., "A 320MHz, 1.5mW at 1.36V CMOS PLL For Microprocessor Clock Generation", IEEE Solid-State Circuits Conference, February 9, 1996, Digest of Technical Papers, 42nd ISSCC96/ SESSION 8 / DIGITAL CLOCKS AND LATCHES / PAPER FA 8.2.	
		YOUNG, et al., "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessor", IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, pp. 1599-1607.	
		NOVOF, et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and + 50 ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30., No. 11, November 1995, pps. 1259-1266.	

Examiner Signature		Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English Translation is attached.

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	10/119,347
				Filing Date	April 7, 2002
				First Named Inventor:	Dave Colleran
				Art Unit	2817
				Examiner Name	Mis, David C.
Sheet	3	**of**	3	Attorney Docket Number	4363P005C

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		MOHAN, et al., "Simple Accurate Expressions for Planar Spiral Inductances", IEEE Journal of Solid-State Circuits, Vol. 34, No. 10, October 1999, pp. 1419-1424.	
		HERSHENSON, "CMOS Analog Circuit Design Via Geometric Programming", A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University, November 2003, 235 pages.	

Examiner Signature		Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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